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TO:	Examiner Jeffrey R. Swearingen	FROM:	Andrew J. Dillon, Reg. No. 29,634
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NOTES/COMMENTS:

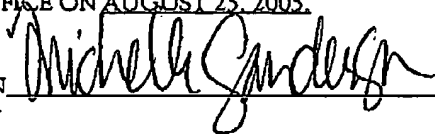
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AUG 25 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

IN RE APPLICATION OF:

**KRAIG A. BOTTEMILLER ET AL.**

SERIAL NO.: 09/876,379

FILED: JUNE 7, 2001

FOR: SYSTEM AND METHOD FOR  
IMPLEMETING A  
COMMUNICATION  
PROFILER

§ ATTY. DOCKET NO.: ROC920000235US1

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§ EXAMINER: JEFFERY R.  
SWEARINGEN

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§ ART UNIT: 2145

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APPEAL BRIEF UNDER 37 C.F.R. §1.192Mail Stop Appeal Briefs - Patents  
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This Brief is submitted in support of the Appeal of the Examiner's final rejection of Claims 1-14 in the above-identified application. A Notice of Appeal was filed in this case on August 4, 2005 and received in the United States Patent and Trademark Office on August 4, 2005. Please charge the fee of \$500.00 due under 37 C.F.R. §1.17(c) for filing the brief, as well as any additional required fees, to IBM Corporation Deposit Account No. 09-0465.

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**REAL PARTY IN INTEREST**

The real party in interest in the present Application is International Business Machines Corporation, the Assignee of the present application as evidenced by the Assignment set forth at reel 011892, frame 0903.

**RELATED APPEALS AND INTERFERENCES**

There are no Appeals or Interferences known to Appellant, the Appellant's legal representative, or assignee, which would be directly affected or have a bearing on the Board's decision in the present Appeal.

**STATUS OF CLAIMS**

Claims 1-14 stand finally rejected by the Examiner as noted in the Final Action dated May 4, 2005.

**STATUS OF AMENDMENTS**

No amendments to the claims have been made subsequent to the final rejections that lead to this appeal.

**SUMMARY OF THE CLAIMED SUBJECT MATTER**

Appellant's Claim 1 recites a communication profiler, for use with a data processing system including a processor and a memory coupled by a system interconnect, wherein the communication profiler includes a control unit that includes an input port coupled to the system interconnect, wherein the control unit receives a collection of data via the input port as a result of a tenure on the system interconnect (Specification, page 4, lines 3-12, Figures 1 and 2). The control unit filters the collection of data from the tenure to obtain specific data requested by a

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user and organizes the specific data as a summary, wherein the control unit filters the collection of data without perturbing the operation of the data processing system (page 4, lines 14-21, Figure 5).

Appellant's Claim 7 recites a data processing system. The data processing system includes a collection of master and slave elements that are coupled to a system interconnect (Specification, page 4, lines 3-12, Figures 1 and 2). Also included in the data processing system is a communication profiler, also coupled to the system interconnect, that receives a collection of data via the input port as a result of a tenure between a master element and a slave element on the system interconnect (Specification, page 4, lines 3-12, Figures 1 and 2). The control unit filters the collection of data from the tenure and retrieves a set of specific data requested by a user and organizes the set of specific data as a summary (page 4, lines 14-21, Figure 5). The control unit filters the collection of data without perturbing the operation of the data processing system (page 4, lines 14-21, Figure 5).

Appellant's Claim 10 recites a host data processing system. The host data processing system includes a host processor, a host memory, and a data processing system, all coupled by a host interconnect (page 5, lines 3-12, Figures 1 and 2). The data processing system includes a collection of master and slave elements that are coupled to a system interconnect (page 4, lines 3-12, Figures 1 and 2). Also included in the data processing system is a communication profiler, also coupled to the system interconnect, that receives a collection of data via the input port as a result of a tenure between a master element and a slave element on the system interconnect (page 4, lines 3-12, Figures 1-2). The control unit filters the collection of data from the tenure and retrieves a set of specific data requested by a user and organizes the set of specific data as a summary (page 4, lines 14-21, Figure 5). The control unit filters the collection of data without perturbing the operation of the data processing system (page 4, lines 14-21, Figure 5).

Appellant's Claim 12 recites a method for gathering hardware performance data. The method includes activating a communication profiler coupled to a system interconnect by setting a control register, which is coupled to a control unit in the communication profiler (page 4, lines 14-21, Figure 5). A system interconnect is monitored for a tenure between a master element and

a slave element of a data processing system, wherein the monitoring further includes filtering the collection of data without perturbing the operation of the data processing system (page 4, lines 14-21, Figure 5). Also, a set of data resulting from the tenure is captured, in response to detecting a tenure on the system interconnect (page 4, lines 14-21, Figure 5). The set of data is organized into a summary (page 4, lines 14-21, Figure 5).

**GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

The Examiner's rejection of Appellant's Claims 1-14 under 35 U.S.C. § 102(e) as being anticipated under *Sidi et al.* (U.S. Patent No. 6,282,562) is to be reviewed on Appeal.

**ARGUMENT**

In the Examiner's Final Action, Claims 1-14 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Sidi*. The Examiner's rejection should be reversed because *Sidi* does not teach or suggest each claimed feature.

Regarding exemplary Claim 1, *Sidi* does not teach or suggest "said control unit filters said collection of data without perturbing the operation of said data processing system."

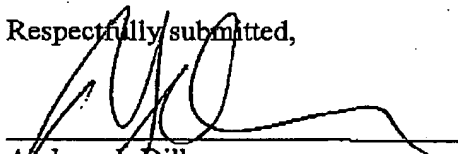
*Sidi* discloses a system and method of observing communications on a data communications system, and in response to the observations, intentionally applying "response time degradation to pedagogically discourage human users of data communications systems from economically disadvantageous interactions" (*Sidi*, col. 2, lines 34-37). Appellant asserts that the application of response time degradation clearly perturbs the operation of the system. The point of observing the communications on the system is to assigned economic values to the communications on the system. The response time of communication that is deemed economically disadvantageous (such as Internet surfing, col. 2, lines 40-50) is degraded, which alters or "perturbs" the operation of the data communications system in order to discourage human users from engaging in those communications.

Accordingly, in light of the preceding argument, Appellant believes that independent Claims 7, 10, and 12 and all dependent claims are not anticipated by *Sidi* and are thus not rendered unpatentable.

CONCLUSION

Appellant has pointed out with specificity the manifest error in the Examiner's rejection, and the claim language which renders the invention patentable over the reference. Appellant, therefore, respectfully requests that this case be remanded to the Examiner with instructions to issue a Notice of Allowance for all pending claims.

Respectfully submitted,



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**CLAIMS APPENDIX**

1. A communication profiler, for use with a data processing system including a processor and a memory coupled by a system interconnect, wherein said communication profiler comprises:

a control unit including an input port coupled to said system interconnect, wherein said control unit receives a collection of data via said input port as a result of a tenure on said system interconnect, wherein said control unit filters said collection of data from said tenure to obtain specific data requested by a user and organizes said specific data as a summary, wherein said control unit filters said collection of data without perturbing the operation of said data processing system.

2. The communication profiler according to claim 1, further comprising:

a profiler interconnect; and

a profiler memory, coupled to said profiler interconnect, wherein said profiler memory stored said summary.

3. The communication profiler according to claim 1, further including:

an output port that can be coupled to an external analyzer to communicate said summary.

4. The communication profiler according to claim 1, further comprising:

a control register, coupled to said control unit, which activates filtering of said collection of data by said control unit.

5. The communication profiler according to claim 1, further including:

a transaction timer, coupled to said control unit, wherein said transaction timer is utilized to record a duration of a operation pending.

6. The communication profiler according to claim 1, further comprising:

a data serializing and transmitting device that serially outputs said summary from said communication profiler, wherein said summary is indicative of normal hardware performance.



7. A data processing system, comprising:  
a system interconnect;  
a plurality of master elements, coupled to said system interconnect;  
a plurality of slave elements, coupled to said system interconnect; and  
a communication profiler, coupled to said system interconnect, further including: a control unit including an input port coupled to said system interconnect, wherein said control unit receives a collection of data via said input port as a result of a tenure between a master element and a slave element on said system interconnect, wherein said control unit filters said collection of data from said tenure and retrieves a set of specific data requested by a user and organizes said set of specific data as a summary, wherein said control unit filters said collection of data without perturbing the operation of said data processing system.
8. The data processing system according to claim 7, wherein said data processing system is a small computer system interface (SCSI) controller.
9. The data processing system according to claim 7, wherein said data processing system is implemented on a single integrated circuit substrate.
10. A host data processing system comprising:  
a host interconnect;  
a host processor coupled to said host interconnect;  
a host memory coupled to said host interconnect;  
a data processing system including a processor and memory coupled by a system interconnect comprising:  
a plurality of master elements, coupled to said system interconnect;  
a plurality of slave elements, coupled to said system interconnect; and  
a communication profiler, coupled to said system interconnect, further including:  
a control unit including an input port coupled to said system interconnect, wherein said control unit receives a collection of data via said input port as a result of a tenure between a master element and a slave element on said system interconnect, wherein said control

unit filters said collection of data from said tenure and retrieves a set of specific data requested by a user and organizes said set of specific data as a summary, wherein said control unit filters said collection of data without perturbing the operation of said data processing system.

11. The host data processing system according to claim 10, further comprising:  
a memory controller, coupled to said host interconnect, utilized to control said host memory.
12. A method for gathering hardware performance data, comprising the steps of:  
activating a communication profiler coupled to a system interconnect by setting a control register, coupled to a control unit in said communication profiler;  
monitoring a system interconnect for a tenure between a master element and a slave element of a data processing system, wherein said monitoring further includes filtering said collection of data without perturbing the operation of said data processing system; and  
capturing a set of data resulting from said tenure and organizing said set of data into a summary, in response to detecting a tenure on said system interconnect.

**EVIDENCE APPENDIX**

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**RELATED PROCEEDINGS APPENDIX**

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